Osaze Y. Shears

Computer Hardware Engineer
Blacksburg, Virginia, 24060
(757) 508-2757 | oshears@vt.edu | oshears | linkedin.com/in/osazeshears

Objective

To research, document, and educate engineers about contemporary digital hardware design technologies and their potential for enhancing emerging devices with artificial intelligence, parallelism, and power efficiency.

Education

Virginia Polytechnic Institute and State University, Blacksburg, Virginia *GPA: 4.0*
Master's of Science in Computer Engineering *May 2022*

- **Research:** Reservoir Computing Accelerator Design for Low-Power, Mobile Computing
- **Lab:** Multifunctional Integrated Circuits and Systems (MICS) Lab
- **Recognitions:** Bradley Research Fellowship • New Horizon Graduate Scholars

George Mason University, Fairfax, Virginia *GPA: 3.97*
Bachelor's of Science in Computer Engineering *May 2018*

- **Recognitions:** Summa Cum Laude • Chairman's Award • Outstanding Academic Performance Award • Honors College

Work Experience

Virginia Polytechnic Institute and State University *Blacksburg, Virginia*
Graduate Research and Teaching Assistant *August 2020 - Present*

- Developed recurrent neural network IP for the BladeRF software defined radio using Intel HLS Compiler and Cyclone V.
- Verified RNN functional correctness using Mentor Graphics ModelSim and high-level synthesis co-simulation.
- Achieved up to 90% accuracy on spectrum occupancy prediction tasks and an error rate of 0.2 on NARMA10.
- Mentored a team of 4 undergraduate students in design and implementation of FPGA machine learning accelerators.
- Presented a mixed-signal ASIC-FPGA neural network at the 2021 International Conference on Computer Aided Design.
- Interfaced FPGA boards to analog circuits using digital-to-analog (DAC) and analog-to-digital (ADC) converters.

Colvin Run Networks, Inc. *McLean, Virginia*
Hardware Engineering Associate *June 2021 - Present*

- Synthesized a Zynq-7000 hardware platform using Xilinx Vivado's IP Integrator to provide an interface for an RTL-SDR.
- Reported potential hardware vulnerabilities based on the Security Annotation for Electronic Design Integration (SA-EDI).
- Presented on ASIC and FPGA design processes, tools, and Colvin Run's supply chain security platform: Copia.
- Researched firmware and hardware vulnerabilities in the NIST National Vulnerability Database (NVD) for Veritech.

BAE Systems *Manassas, Virginia*
Digital Logic Design Engineer *May 2018 - July 2020*

- Constructed UVM testbenches to perform functional verification for 10+ IP cores, including PCI, I2C, UART, and SPI.
- Generated wafer-level and module-level test patterns to verify SerDes and MBIST IP functions on the RAD5545 SoC.
- Mentored a team of interns in the design of memory test and repair programs using C++ and a JTAG controller.
- Presented automated MBIST test and insertion research to the Virginia Microelectronics Consortium (VMEC).

Publications

O. Shears, K. Bai, L. Liu and Y. Yi, "A Hybrid FPGA-ASIC Delayed Feedback Reservoir System to Enable Spectrum Sensing/Sharing for Low Power IoT Devices ICCAD Special Session Paper," *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2021, pp. 1-9, doi: 10.1109/ICCAD51958.2021.9643536.

Technical Skills

Languages SystemVerilog/Verilog • VHDL • Python • C/C++ • Java • MATLAB • Universal Verification Methodology (UVM)
Software Vivado • Vitis • Quartus Prime • ModelSim • Questa • High-Level Synthesis • GNU Radio • Xcelium